CLAIMS

1. A method of fabricating a TFT comprising:

etching a base layer structure (9) on a substrate (1) so as to form a gate (4) with inclined side edges (4a, 4b) that extend towards an apex region (12),

depositing material to form a channel layer (6) over the inclined side edges and the apex region,

depositing conductive material (8) over the channel layer so as to cover the apex region and the side edges,

applying a layer of masking material (14) over the conductive material (8), such that the conductive material in the apex region protrudes through and upstands from the masking material, and

selectively etching the conductive material that protrudes through the masking material in the apex region such as to provide separate source and drain regions (8a, 8b) overlying the inclined edges.

2. A method according to claim 1 including applying the masking material (14) to cover the apex region and then selectively removing the masking material so that the conductive material (8) in the apex region (12) protrudes through and upstands from the masking material.

3. A method according to claim 2 wherein the masking material comprises a photo resist (14), and including spinning the substrate to cover the conductive material with the photo resist.

4. A method according to claim 3 including selectively etching the photo resist (14) to expose the apex region (12).

5. A method according to any preceding claim wherein the etching of the base layer structure (9) is carried out such that a tip (13) is formed in the apex region, having a radius of a few nanometres.

6. A method of fabricating a TFT comprising:

etching a base layer structure (9) on a substrate so as to form a base region (4) with inclined side edges (4a, 4b) which extend towards an apex region (12) that includes a tip (13) of a radius of a few nanometres,

depositing material to form a channel layer (6) over apex region and the inclined side edges,

depositing conductive material (8) over the channel layer, and

selectively etching the conductive material in the apex region such as to provide separate source and drain regions (8a, 8b) overlying the inclined edges, and

providing a gate (4) in said base region.

7. A method according to claim 5 or 6 including removing the tip (13) before depositing the channel layer.

8. A method according to any preceding claim including depositing an electrically insulating layer (5) over the gate, and depositing the channel layer (6) over the insulating layer.

9. A method according to claim 8 including depositing a doped semiconductor layer (7) over the channel layer, and depositing the conductive material in a layer over the doped semiconductor layer.

10. A method according to any preceding claim including carrying out the etching of the base layer structure (4) such that the side edges are inclined at angle of less than 90 degrees.

11. A method according to any preceding claim wherein the etching of the base layer structure includes masking a region of the base layer structure, and etching the base layer structure such that a ridge structure is formed from the base layer structure in the masked region.

12. A method according to any preceding claim wherein the base layer structure comprises a layer of conductive material overlying a layer of insulating material and the etching of the base layer structure is carried out so as to form a ridge structure from the base layer structure.

13. A TFT fabricated by a method as claimed in any preceding claim.

14. A device including a TFT according to claim 13.

15. An AMLCD including a plurality of TFTs fabricated by a method as claimed in any one of claims 1 to 13.

16. A TFT comprising a substrate (1), a gate (4) overlying the substrate and having side edges (4a, 4b) inclined towards one another, a channel region overlying the gate (6), and source and drain regions (8a, 8b) overlying said side edges respectively, wherein the gate has been formed on the substrate by an etching process that involved formation of a tip (13) in an apex region (12) between the side edges of a radius of a few nanometres.

17. A TFT according to claim 16 wherein the tip (13) was removed before the channel region was applied.

18. A TFT according to claim 16 or 17 wherein the gate is overlaid by a layer of insulating material (5), the channel region (6) overlies the insulating material, a layer of doped semiconductor material (7) overlies the channel region, and a layer of conductive material (8) from which said source and drain regions have been formed, overlies the doped semiconductor material.

19. A TFT according to any one of claims 16 to 18 wherein the channel region (6) comprises intrinsic amorphous silicon.

20. A TFT according to claim 18 wherein the insulating layer comprises (5) silicon nitride.

21. A TFT according to claim 18 wherein the doped semiconductor material (7) comprises n doped silicon.